Amendments to the Claims:

Following is a listing of all claims in the present application, which listing supersedes all previously presented claims:

Listing of Claims:

Claims 1-3 (Canceled).

4. (Currently Amended) A method of forming a self-aligned buried contact pair, comprising:

depositing a lower layer on a substrate having diffusion regions;

forming a plurality of bit lines having bit line sidewall spacers on the lower layer;

forming an upper interlayer dielectric (ILD) layer on the lower layer, the plurality of bit lines and bit line sidewall spacers;

etching the ~~upper ILD layer and~~ the lower layer to expose a pair of adjacent diffusion regions in the substrate simultaneously;

forming a pair of buried contact pads on the exposed pair of adjacent diffusion regions in the substrate; and

forming a capacitor on each of the pair of buried contact pads.

5. (Previously Presented) The method as claimed in claim 46, wherein the oxide layer is formed using a thermal oxidation process.

6. (Previously Presented) The method as claimed in claim 4, wherein the upper ILD layer is deposited using a chemical vapor deposition (CVD) process.

7. (Previously Presented) The method as claimed in claim 6, further comprising: planarizing the upper ILD layer after depositing the upper ILD layer.

8. (Previously Presented) The method as claimed in claim 7, wherein the upper ILD layer is planarized using a chemical mechanical polishing (CMP) process.

9. (Previously Presented) The method as claimed in claim 4, wherein forming the pair of buried contact pads comprises:

depositing a pad layer on the pair of exposed diffusion regions; and

planarizing the pad layer and the upper ILD layer to expose the plurality of bit lines.

10. (Original) The method as claimed in claim 9, wherein the pad layer is deposited using a CVD process.

11. (Previously Presented) The method as claimed in claim 9, wherein the pad layer and the upper ILD layer are planarized using a CMP process.

12-16 (Canceled).

17. (Previously Presented) The method as claimed in claim 35, further comprising:

forming a first direct contact pad in the lower ILD layer diffusion region adjacent the pair of adjacent diffusion regions; and

forming a second direct contact pad in the intermediate ILD layer over the first direct contact pad.

18. (Previously Presented) The method as claimed in claim 17, wherein the lower ILD layer is formed by a CVD process.

19. (Previously Presented) The method as claimed in claim 17, wherein the intermediate ILD layer is formed by a CVD process.

20. (Previously Presented) The method as claimed in claim 17, wherein the upper ILD layer is formed by a CVD process.

21. (Previously Presented) The method as claimed in claim 17, wherein forming the first buried contact pads and first direct contact pads comprises:

patterning the lower ILD layer;

etching the lower ILD layer;

depositing a first pad layer over the etched lower ILD layer; and

planarizing the first buried contact pads, the first direct contact pads, and the lower ILD layer.

22. (Previously Presented) The method as claimed in claim 21, wherein planarizing the first buried contact pads, the first direct contact pads, and the lower ILD layer is performed by a method selected from the group consisting of a CMP and an etch-back process.

23. (Previously Presented) The method as claimed in claim 17, wherein forming the second direct contact pads comprises:

etching the intermediate ILD layer;

depositing a conductive layer over the etched intermediate ILD layer; and

planarizing the conductive layer to expose the intermediate ILD layer so that the conductive layer material only remains in the etched portion of the intermediate ILD layer.

24. (Original) The method as claimed in claim 23, wherein the conductive layer is deposited using a CVD process.

25. (Original) The method as claimed in claim 23, wherein the conductive layer is planarized using a CMP process.

26. (Previously Presented) The method as claimed in claim 17, wherein each of the plurality of bit lines comprises:

a bit line barrier metal formed on the intermediate ILD layer;

a WSi layer formed on the bit line barrier metal; and

a bit line mask formed on the WSi layer.

27. (Currently Amended) The method as claimed in claim 17, further comprising:

planarizing the ~~third~~ upper ILD layer after depositing the upper ILD layer.

28. (Previously Presented) The method as claimed in claim 27, wherein the upper ILD layer is planarized using a CMP process.

29. (Previously Presented) The method as claimed in claim 17, wherein forming the second buried contact pads comprises:

depositing a third pad layer on the exposed pair of adjacent first buried contact pads; and

planarizing the third pad layer and the upper ILD layer to expose the plurality of bit lines.

30. (Original) The method as claimed in claim 29, wherein the third pad layer is deposited using a CVD process.

31. (Original) The method as claimed in claim 29, wherein the third pad layer is planarized using a CMP process.

32-34 (Canceled).

35. (Currently Amended) The method as claimed in claim 4, wherein the lower layer is a lower ILD layer further comprising:

forming the pair of buried contact pads includes forming a pair of first buried contact pads in the lower ILD layer;

forming an intermediate ILD layer on the lower ILD layer and the first buried contact pads;

forming the plurality of bit lines on the lower ILD layer includes forming the plurality of bit lines on the intermediate ILD layer;

forming [[an]] the upper ILD layer on the intermediate ILD layer, the plurality of bit lines and bit line sidewall spacers;

etching the upper ILD layer and the intermediate ILD layer to expose the pair of first buried contact pads simultaneously;

forming second buried contact pads on the exposed pair of first buried contact pads; and

forming the capacitor includes forming the capacitor on each of the second buried contact pads.

36. (Previously Presented) The method as claimed in claim 35, wherein the lower ILD layer is formed by a CVD process.

37. (Previously Presented) The method as claimed in claim 35, wherein the intermediate ILD layer is formed by a CVD process.

38. (Previously Presented) The method as claimed in claim 35, wherein the upper ILD layer is formed by a CVD process.

39. (Previously Presented) The method as claimed in claim 35, further comprising: planarizing the upper ILD layer after depositing the upper ILD layer.

40. (Previously Presented) The method as claimed in claim 39, wherein the upper ILD layer is planarized using a CMP process.

41. (Previously Presented) The method as claimed in claim 35, wherein forming the first buried contact pads comprises:

patterning the lower ILD layer;

etching the lower ILD layer;

depositing a first pad layer over the lower ILD layer; and

planarizing the first pad layer to expose the lower ILD layer so that the first pad layer only remains in the etched portion of the lower ILD layer.

42. (Original) The method as claimed in claim 41, wherein the first pad layer is planarized using a method selected from the group consisting of a CMP process and an etch-back process.

43. (Previously Presented) The method as claimed in claim 35, wherein forming the second buried contact pads comprises:

depositing a second pad layer on the exposed pair of adjacent first buried contact pads; and

planarizing the second pad layer and the upper ILD layer to expose the plurality of bit lines.

44. (Original) The method as claimed in claim 43, wherein the second pad layer is deposited using a CVD process.

45. (Original) The method as claimed in claim 43, wherein the second pad layer is planarized using a CMP process.

46. (Previously Presented) The method as claimed in claim 4, wherein the lower layer is an oxide layer.